Abstract

A family of embodiments of a new class of CMOS VLSI computer multiplier circuits that are simpler to fabricate, smaller, faster, more efficient in their use of power, and easier to scale in size than the prior art. The normal binary adder circuit unit is replaced by the innovative shift switch circuit unit. Use of the shift switch circuit sharply reduces fluctuations of power caused by plurality variations in the bit representations of the input, intermediate and output numbers. Reduced-scale devices are used in shift-switch pass-transistor signal restoration circuits, significantly reducing the size, power demand, and power dissipation of internal circuitry, in contrast to ordinary multiplier design. The simplicity of the circuit design allows multiplier partial-product reduction in fewer logic stages than existing comparable designs allow, showing speed improvement over such designs. The circuit design simplicity and the use of reduced-scale devices require less VLSI area than existing designs need, facilitating integration in VLSI microprocessors. Modular circuit organization simplifies scaling for larger operands without the circuit complications of existing designs. The design includes a critical flip of the physical layout of the partial-product matrix at each size level, simplifying the layout of traces in the circuit at all size scales. Finally, the application of reconfigurable design principles to the easily-scaled layout reduces significantly the mean demand for computing resources over a wide range of multiplication bit-width scales, as compared to existing designs. Overall, the orchestrated integration of these diverse design innovations makes possible the implementation of simpler, faster, smaller, more efficient, more flexible, and easier-to-build VLSI multiplication circuits than the current art reveals.